AMENDMENTS

IN THE SPECIFICATION:

Please replace the paragraph beginning on page 12, line 4, with the paragraph as follows below.

Referring now to the figures, Fig. 2 of the present invention illustrates a cross-sectional view of an exemplary multi-polar ESC 100 according to one aspect of the invention, wherein the ESC is operable to support and cool a substrate 105 residing thereon. The substrate 105, for example, is generally characterized by a diameter D and a bottom surface 107, wherein the bottom surface has a first surface area (not shown) associated therewith. It should be noted that the electrostatic chuck 100 of Fig. [[1]] 2 is illustrated macroscopically for simplicity, however, subsequent Figures (*e.g.*, Figs. 5, 6 and others) are provided which illustrate exemplary blown-up views of the electrostatic chuck 100 in further detail. Furthermore, it should be noted that wherein a cooling of the wafer or substrate is described, a heating of the substrate may alternatively be performed, and such heating is further contemplated as falling within the scope of the present invention.

Please replace the paragraph beginning on page 23, line 15, with the paragraph as follows below.

According to still another exemplary aspect of the present invention, the second electrically conductive layer 165 further comprises a plurality of electrically conductive vertical interconnects 170. The vertical interconnects 170, for example, electrically connect the first electrically conductive layer 125 and the second electrically conductive layer [[145]] 165. A plurality of electrodes 175, for example, are further electrically connected to the second electrically conductive layer 165, therein electrically connecting the first electrically conductive layer 125 to the plurality of electrodes *via* the plurality of vertical interconnects 170. The plurality of vertical interconnects 170 may comprise, for example, a plurality of vias 180 associated with the semiconductor platform 120, wherein the plurality of vias generally extend from the top surface 127 to the bottom surface 168 of the semiconductor platform. The plurality of vias 180, therefore, electrically connect each portion 130 of the first electrically conductive layer 125 to the respective portion 167 of the second electrically conductive layer 165. Each portion 130 and 167 of the first electrically conductive layer 125 and second electrically conductive layer 165, respectively, may be electrically connected, for example, by one or more of the plurality of vias 180 (*e.g.,* portion 130A is electrically connected to portion 167A through one or more vias 180A). As Illustrated in Fig. 11, for example, the plurality of vias 180 are generally oriented about the semiconductor platform 120 such that the clamping plate 110 is substantially thermally and electrically balanced.

Please replace the paragraph beginning on page 26, line 19, with the paragraph as follows below.

Referring again to Fig. [[8]] 11, according to another exemplary aspect of the invention, a plurality of lift pins 210 are operatively coupled to the clamping plate 110, wherein the plurality of lift pins 210 are operable to vertically translate the substrate 105 of Fig. 2 between a processing position (not shown) proximate to the clamping plate 110 and a loading position (not shown) generally above the clamping plate (*e.g.*, approximately 1-2 mm above the clamping plate). The lift pins 210 of Fig. 11, for example, are comprised of quartz, silicon carbide, or a ceramic material, wherein contamination of the substrate 105 from the lift pins during processing is minimized. Furthermore, the lift pins 210 have a generally small diameter (*e.g.*, 1 or 2 mm) that will significantly limit a volume occupied by the lift pins within the electrostatic chuck 100 of Fig. 2 when the pins are in the processing position. Minimizing the volume occupied by the lift pins 210 while in the processing position is advantageous, wherein the backside pressure can be quickly modified.